CLAIMS

Please amend the claims as follows:

1-27. (Cancelled)

28. (Presently amended) A system for distributing content comprising:

a semiconductor memory array that stores content;

a first stream server module comprising;

a first stream server processor that requests content and encodes it;

a first media access controller that receives the encoded content and serializes the received encoded content for physical layer transport; and

a first media interface module that formats the serialized encoded content from the first media access controller into a format for a physical interface;

a second stream server module;

a backplane interface that forwards content to the semiconductor array; and

an interconnect connected to the memory, ~~and~~ the first stream server module, ~~and~~ the second stream server module and the backplane interface comprising;

an address bus that is larger than 32 bits wide coupled between the first stream server module and the semiconductor memory array and coupled between the second stream server module and semiconductor memory array and coupled between the backplane interface and the semiconductor memory that carries content addresses;

a data bus coupled between first stream server module and the semiconductor memory array and coupled between the second stream server module and the semiconductor memory array and coupled between the backplane interface and the semiconductor array that carries content; and

an arbitrator that determines which of the first stream server module and the second stream server module may access either the address bus or the data bus based and which of the first stream server module and the second stream server module has priority;

wherein the interconnect forwards content from the backplane interface to the semiconductor memory and forwards content from the semiconductor memory to the first stream server module in a time frame relative to the latency of the semiconductor memory.

29. (Previously presented) The system of claim 28 wherein the second stream server module comprises:

a second stream server processor that requests content and encodes it;

a second media access controller that receives the encoded content and serializes the received encoded content; and

a second media interface module that formats the serialized encoded content from the second media access controller into a format for a physical interface.

30. (Previously presented) The system of claim 28 wherein the first stream server module further comprises:

a control processor that receives control packets that control how the content is output by the first stream server processor.

31. (Previously presented) The system of claim 28 wherein the first stream server processor further comprises:

a first stream controller comprising:

an address generator that generates content addresses that are forwarded to the address bus;

a payload data buffer that receives content from the data bus;

a control data buffer that receives control data; and

a protocol stream encoder/decoder for receiving content from the payload data buffer and control data from the control data buffer.

32. (Previously presented) The system of claim 31 wherein the protocol stream encoder/decoder further comprises:

at least two protocol encoder logic modules that receives the content and encode the received content into at least two different protocols; and

a protocol select logic module that receives the content and forwards it to one of the at least two protocol encoder logic modules.

33. (New) The system of claim 28 wherein the interconnect forwards content from the semiconductor memory to the first stream server and forwards content from the

semiconductor memory to the second stream server module in the time frame relative to the latency of the semiconductor memory.